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(54) Title: OVERLAY METROLOGY MARK

(57) Abstract: An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with and in particular developed on a first layer and a second mark portion associated with and in particular developed on the surface of a second layer, wherein each mark portion comprises a single two dimensional generally orthogonal array of individual test structures. A method of marking and a method of determining overlay error are also described.